

Appln. No. 10/032,185  
Amendment dated December 22, 2005  
Reply to Office Action of September 27, 2005

**Amendments to the Claims:**

Please amend claims 1 and 3 as follows. The following listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1 (Currently Amended). A circuit for generating dot clock pulses utilized for an image-forming apparatus having an image-writing section, comprising:

a digital-delay dot clock adjusting section to generate  
5 first dot clock pulses having a predetermined number of pulses within a predetermined time interval at a constant exposing range of said image-writing section for making a correction against a deviation expanded or contracted, wherein each period of said first dot clock pulses is slightly increased or reduced by  
10 changing a successive selection for a plurality of delayed clock pulses, which are generated successively in slightly different delay times by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times; and

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a jitter suppressing section to suppress a jitter component  
15 included in said first dot clock pulses, wherein said jitter  
suppressing section divides said first dot clock pulses to  
generate second dot clock pulses, and then, multiplies said  
second dot clock pulses to generate said dot clock pulses.

Claim 2 (Original). The circuit of claim 1,

wherein said jitter suppressing section comprises,

a voltage controlled oscillator to generate said second  
dot clock pulses;

5 a first divider to divide said first dot clock pulses  
outputted by said digital-delay dot clock adjusting section;

a second divider to divide said second dot clock pulses  
generated by said voltage controlled oscillator; and

a phase comparator to perform a frequency-phase  
10 comparison between first divided dot clock pulses outputted by  
said first divider and second divided dot clock pulses outputted  
by said second divider to output a comparison result voltage, and

wherein said phase comparator feedbacks said comparison  
result voltage to said voltage controlled oscillator so as to  
15 constitute a phase locked loop, serving as a flywheel oscillator  
to disperse said jitter component.

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Claim 3 (Currently Amended). An image-forming apparatus,  
comprising:

an image-bearing member to bear a electrostatic latent image  
and/or a toner image on it;

5 an image-writing device to scan a surface of said  
image-bearing member with a scanning-light deflected by a  
rotating polygon mirror;

a modulating section that performs a pulse width modulation  
or a light-intensity modulation of dot clock pulses in response  
10 to image data to generate a scanning-light modulation signal to  
be fed to said image-writing device;

a developing section that develops said electrostatic latent  
image, formed on said image-bearing member by said  
scanning-light, to form said toner image as a visual image;

15 a transferring section to transfer said toner image borne on  
said image-bearing member to a transfer material;

a fixing section to fix said toner image, transferred to  
said transfer material, onto said transfer material;

a digital-delay dot clock adjusting section to generate  
20 first dot clock pulses having a predetermined number of pulses  
within a predetermined time interval at a constant exposing range

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of said image-writing section for making a correction against a deviation expanded or contracted, wherein each period of said first dot clock pulses is slightly increased or reduced by  
25 changing a successive selection for a plurality of delayed clock pulses, which are generated successively in slightly different delay times by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times; and  
a jitter suppressing section to suppress a jitter component  
30 included in said first dot clock pulses, wherein said jitter suppressing section divides said first dot clock pulses to generate second dot clock pulses, and then, multiplies said second dot clock pulses to generate said dot clock pulses.

Claim 4 (Original). The image-forming apparatus of claim 3, wherein said jitter suppressing section comprises,

a voltage controlled oscillator to generate said second dot clock pulses;

5 a first divider to divide said first dot clock pulses outputted by said digital-delay dot clock adjusting section;

a second divider to divide said second dot clock pulses generated by said voltage controlled oscillator; and

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a phase comparator to perform a frequency-phase  
10 comparison between first divided dot clock pulses outputted by  
said first divider and second divided dot clock pulses outputted  
by said second divider to output a comparison result voltage, and  
wherein said phase comparator feedbacks said comparison  
result voltage to said voltage controlled oscillator so as to  
15 constitute a phase locked loop, serving as a flywheel oscillator  
to disperse said jitter component.

Claim 5 (Original). The image-forming apparatus of claim 3,  
wherein said image-forming apparatus forms a color image  
based on a plurality of primary colors, and said image-writing  
device, said digital-delay dot clock adjusting section and said  
5 jitter suppressing section are provided corresponding to each of  
said primary colors.

Claim 6. The image-forming apparatus of claim 3,  
wherein said image-forming apparatus forms an obverse image  
and a reverse image on both sides of said transfer material, so  
that a position of said obverse image coincides with a position  
5 of said reverse image.